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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,191	06/02/2000	Adrian J. Isles	HDCA1003USO	6083

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VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 MARKET STREET, SUITE 540
SAN FRANCISCO, CA 94105

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	9

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,191	ISLES, ADRIAN J.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-51 of U.S. Application 09/586,191, originally filed on 06/02/2000 and amended in paper #8 on 12/8/03, are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-11, 23, 29-31, 45-47, and 50-51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 23, and 29 recite the limitation "... wherein the lookup table is used to represent the physical memory with a description of the electronic design". This phrase is indefinite. It is not clear from the limitation whether:

   a. the look-up table, with the description of the electronic design, is used to represent the physical memory.
   b. the look-up table represents a physical memory, where the physical memory comes with a description of the electronic design.
   c. some other interpretation of this limitation is correct.

4. Claims 12-13, and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 recites the limitation "... wherein the lookup table is used to represent the combinational block with a description of the electronic design". This phrase is indefinite. It is not clear from the limitation whether:
    a. the look-up table, with the description of the electronic design, is used to to represent the combinational block.
    b. the look-up table represents a combinational block, where the combinational block comes with a description of the electronic design.
    c. some other interpretation of this limitation is correct.
5. Claims 14-22, 34-41, and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 14 and 34 recite the limitation "... wherein the memory model is used to represent the physical memory with a description of the electronic design". This phrase is indefinite. It is not clear from the limitation whether:
    a. the memory model, with the description of the electronic design, is used to represent the physical memory.
    b. the memory model represents a physical memory, where the physical memory comes with a description of the electronic design.
    c. some other interpretation of this limitation is correct.

6. Applicant states in the "Summary of the Invention" (specification, p.4) that "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table." Examiner is interpreting the claims in light of this statement in the specification.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The prior art used for these rejections is as follows:

9. Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching". © 1996. (Henceforth referred to as "**Weems**").

10. Murgai, R. et al. "Logic Synthesis for Programmable Gate Arrays". 27th ACM/IEEE Design Automation Conference. 1991.

11. Bayoumi, M. et al. "A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications." IEEE Transactions on Circuits and Systems. Vol. 34, Issue 6, June 1997. pp.604-616. (Henceforth referred to as "**Bayoumi**").

12. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

13. Claims 1-22, and 29-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weems in view of Murgai.

14. In regards to Claim 1, Weems teaches the following limitations:

1. A method for modeling a physical memory for use in an electronic design, the method comprising the steps of:

modeling a memory write operation using a lookup table; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

modeling a memory read operation using the lookup table.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

wherein the lookup table is used to represent the physical memory with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or

VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

15. In regards to Claim 2, Weems teaches the following limitations:

2. The method of claim 1, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits corresponding to write data written to the physical memory at the write address; and

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

16. In regards to Claim 3, Weems teaches the following limitations:

3. The method of claim 2, wherein the step of modeling a memory write operation further comprises the step of:

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

17. In regards to Claim 4, Weems teaches the following limitations:

4. The method of claim 2, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

18. In regards to Claim 5, Weems teaches the following limitations:

5. The method of claim 1, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

19. In regards to Claim 6, Weems teaches the following limitations:

6. The method of claim 5, wherein the step of creating a memory read operation further comprises the step of:

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

20. In regards to Claim 7, Weems teaches the following limitations:

7. The method of claim 5, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary data value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary data value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

21. In regards to Claim 8, Weems teaches the following limitations:

8. The method of claim 7, wherein the arbitrary data value represents an initial value of the plurality of read data bits after an initialization step.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

22. In regards to Claim 9, Weems teaches the following limitations:

9. The method of claim 1, wherein a number of entries in the lookup is limited by a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

computing a total number of memory operations that can be performed per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

23. In regards to Claim 10, Weems teaches the following limitations:

10. The method of claim 9, further comprising the steps of:
determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

24. In regards to Claim 11, Weems teaches the following limitations:

11. The method of claim 1, further comprising the step of:
initializing a plurality of bits in a data field of an entry of the lookup table to an initial value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

25. In regards to Claim 12, Weems teaches the following limitations:

12. A method for modeling an uninterpreted combinational block of an electronic circuit design in a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the method comprising the steps of:

initializing the lookup table;

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

wherein the lookup table is used to represent the combinational block with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

26. In regards to Claim 13, Weems teaches the following limitations:

> 13. The method of claim 12, further comprising the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

27. In regards to Claim 14, Weems teaches the following limitations:

> 14. A method for modeling a physical memory in an electronic circuit design, the method comprising the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation in a memory model to represent a memory write operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

the memory model is used to represent the physical memory with a description of the electronic circuit design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or

VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

28. In regards to Claim 15, Weems teaches the following limitations:

> 15. The method of claim 14, wherein the plurality of write data bits are written to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

29. In regards to Claim 16, Weems teaches the following limitations:

> 16. The method of claim 14, further comprising the following steps if the entry does not contain the plurality of write address bits in the address

field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

30. In regards to Claim 17, Weems teaches the following limitations:

17. The method of claim 14, further comprising the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation in the memory model to represent a memory read operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

31. In regards to Claim 18, Weems teaches the following limitations:

18. The method of claim 17, wherein the plurality of read data bits from a data field of the entry is returned if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

32. In regards to Claim 19, Weems teaches the following limitations:

19. The method of claim 17, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

33. In regards to Claim 20, Weems teaches the following limitations:

20. The method of claim 14, wherein the memory model comprises a lookup table.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

34. In regards to Claim 21, Weems teaches the following limitations:

21. The method of claim 20, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining a number of write ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

computing a total number of memory operations that can be performed

per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

35. In regards to Claim 22, Weems teaches the following limitations:

22. The method of claim 21, further comprising the steps of:
determining a number of memory read operations in a property; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

36. In regards to Claim 29, Weems teaches the following limitations:

29. A processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory, the method comprising the steps of:

modeling a memory write operation using a lookup table; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

modeling a memory read operation using the lookup table.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

wherein the lookup table is used to represent the physical memory with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where

memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

37. In regards to Claim 30, Weems teaches the following limitations:

30. The processor readable storage medium of claim 29, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

38. In regards to Claim 31, Weems teaches the following limitations:

31. The processor readable storage medium of claim 30, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

39. In regards to Claim 32, Weems teaches the following limitations:

32. The processor readable storage medium of claim 29, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

40. In regards to Claim 33, Weems teaches the following limitations:

33. The processor readable storage medium of claim 32, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and the valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

41. In regards to Claim 34, Weems teaches the following limitations:

34. An apparatus for creating a memory model for use in modeling an electronic design having a physical memory, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation using a memory model;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation using the memory model;
determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

wherein the memory model is used to represent the physical memory with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

42. In regards to Claim 35, Weems teaches the following limitations:

35. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

43. In regards to Claim 36, Weems teaches the following limitations:

36. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

44. In regards to Claim 37, Weems teaches the following limitations:

37. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

45. In regards to Claim 38, Weems teaches the following limitations:

38. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

writing the plurality of write data bits to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

46. In regards to Claim 39, Weems teaches the following limitations:

39. The apparatus of claim 34, wherein the memory model comprises a lookup table.

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

47. In regards to Claim 40, Weems teaches the following limitations:

40. The apparatus of claim 39, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining a number of write ports of the physical memory;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

computing a total number of memory operations that can be performed by the electronic design per clock cycle; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

48. In regards to Claim 41, Weems teaches the following limitations:

41. The apparatus of claim 40, further comprising the steps of:

determining a number of memory read operations in a property, the property being a set of behaviors of the physical memory; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations in a property to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

49. In regards to Claim 42, Weems teaches the following limitations:

42. An apparatus for creating a model of an uninterpreted combinational block of an electronic circuit design using a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

wherein the lookup table is used to represent the uninterrupted combinational block with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or

VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

50. In regards to Claim 43, Weems teaches the following limitations:

> 43. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the step of: initializing the lookup table.
> (Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

51. In regards to Claim 44, Weems teaches the following limitations:

> 44. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry

wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

52. In regards to Claim 45, Weems does not expressly teach the following limitations:

45. The method of Claim 1, further comprising:

using the description and the lookup table with a software tool to simulate the electronic design

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description'

(like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

53. In regards to Claim 46, Weems does not expressly teach the following limitations:

46. The method of claim 1, wherein the lookup table is a software data structure that is used to represent the physical memory and the description of the electronic design is a hardware description language description of the electronic design.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description'

(like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

54. In regards to Claim 47, Weems does not expressly teach the following limitations:

47. The method of claim 1, wherein the lookup table is used to represent the physical memory with a description of the electronic design by replacing a portion of a gate level description of the electronic design relating to the physical memory with the lookup table.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description'

(like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

55. In regards to Claim 48, Weems does not expressly teach the following limitations:

48. The method of claim 12, wherein the lookup table is a software data structure that is used to represent the uninterpreted combinational block and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description'

(like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

56. In regards to Claim 49, Weems does not expressly teach the following limitations:

49. The method of claim 14, wherein the memory model is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description'

(like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

57. In regards to Claim 50, Weems does not expressly teach the following limitations:

50. replacing a portion of the memory model relating to the physical memory with the lookup table.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

58. In regards to Claim 51, Weems does not expressly teach the following limitations:

51. The method of claim 12, wherein the lookup table is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

59. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayoumi in view of Murgai.

60. In regards to Claim 23, Bayoumi teaches the following limitations:

23. A method for modeling an electronic circuit design having a physical memory, the physical memory being represented by a lookup table, the method comprising the steps of:

creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

creating a hardware description language description of the memory model and a plurality of components of the electronic circuit design;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

synthesizing a gate level description of the memory model and the plurality of components of the electronic circuit design;
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

verifying operation of the electronic circuit design using a set of properties.
(Bayoumi, especially: pp.605-607, "III. RNS-Based Systems in the VLSI Medium", "IV. A Look-Up Table Layout Methodology")

However, Bayoumi does not expressly teach the intended use claimed by the Applicant in the following limitation:

the lookup table representing the physical memory with a description of the electronic design.

Examiner has interpreted this ambiguous limitation in light of the disclosure in the "Summary of the Invention" (specification, p.4), which states that (emphasis added) "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table."

Murgai teaches (See Abstract, 1.Introduction, and 2.1 TLU Architectures) the use of "'automatic tools' that take 'high level descriptions' (like equations or VHDL description) of a circuit and synthesize onto these architectures [Programmable Devices]."

Moreover, Murgai also teaches that Programmable Gate Array (PGA) devices consist of arrays of identical logic blocks, and that one of these block structures are Table Look-Ups (TLU).

Therefore, Murgai teaches that equations or VHDL are used to "model" the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Weems with those of Mugai because "Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations or VHDL description) of a circuit and synthesize onto these archtectures." (Murgai, 1.Introduction).

61. **Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayoumi in view of Murgai, and further in view of Weems.**

62. In regards to Claim 24, Bayoumi does not expressly teach the following limitations regarding the behavior of a lookout table. Weems, however, does teaches the following limitations:

24. The method of claim 23, wherein the step of creating the memory model comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and a valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to the data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

Bayoumi teaches "selecting the most efficient layout" for "developing a lookout table" in VLSI (see Bayoumi Abstract).

Weems teaches the behavior of the finished "Basic Cache Structures" (see Weems, p.3) and metrics for caches on existing processors (see Weems, pp.9-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bayoumi with those of Weems, because doing so would make it easier to analyze the design produced by Bayoumi, and would also make it easier to compare that design to existing designs.

63. In regards to Claim 25, Weems teaches the following limitations:

25. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

64. In regards to Claim 26, Weems teaches the following limitations:

26. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

65. In regards to Claim 27, Weems teaches the following limitations:

27. The method of claim 23, wherein the upper limit represents a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a total number of memory read ports in the physical memory;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

determining a total number of memory write ports in the physical memory;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

computing a total number of memory operations that can be performed per clock cycle;
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

66. In regards to Claim 28, Weems teaches the following limitations:

28. The method of claim 27, further comprising the steps of:

determining a number of memory read operations performed in the set of properties; and
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

adding the number of memory read operations performed in the set of properties to the total number of memory operations.
(Weems, especially: p.2, discussion of "hit ratio"; and p.15, 3rd para.)

Response to Amendment

67. Examiner acknowledges Applicant's amendment to the descriptions of Figs.2-5 on p.6 of the specification. No new matter has been added. Examiner has also found Applicant's arguments regarding the figures to be persuasive. Moreover, the original copy of Fig.6 has been located in the case. Examiner has withdrawn all objections to the drawings.

68. Applicants unpersuasively argue (paper #8, p.18) that Claims 5-7, 24, and 32-33 have been amended to "correct minor typographical errors" and are "not made for any reason related to patentability or in response to any rejection or objection issued by the Examiner." Examiner finds that there is a substantive difference in the scope of the claims when the word "creating" is replaced with the "modeling", as in Claims 5-7, and 32-33. These words are not equivalent. The same applies to replacing the term "memory model" with the term "lookup table". These terms are also not equivalent.

69. In regards to Applicant's arguments (paper #8, pp.19-20) regarding the rejections of Claims 1-22 and 29-44 as being anticipated by Weems, applicant is arguing a feature ("modeling physical memories in an electronic design") that has only

been amended into the claim with paper #8. Examiner has modified the rejection, as necessitated by the amendment.

70. In regards to Applicant's arguments (paper #8, pp.25-26) regarding the rejections of Claim 23 as being anticipated by Bayoumi, applicant is arguing a feature ("the lookup table representing the physical memory with a description of the electronic circuit design") that has only been amended into the claim with paper #8. Examiner has modified the rejection, as necessitated by the amendment.

71. In regards to Applicant's arguments (paper #8, p.25-26) regarding the rejections of Claims 24-28 as being unpatentable over Bayoumi in view of Weems, applicant is arguing a feature ("creating the lookup table ...") that has only been amended into the claim with paper #8. Examiner has modified the rejection, as necessitated by the amendment.

Conclusion

72. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

73. Seawright, J. U.S. Patent 6,539,477.

74. Schneider, C. "A Parallel / Serial Trade-Off Methodology for Look-up Table Based Decoders." Proc. of the 34th Annual Conf. on Design Automation Conf. 1997. 1997. pp.498-503.

75. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

February 20, 2004